FIG.1

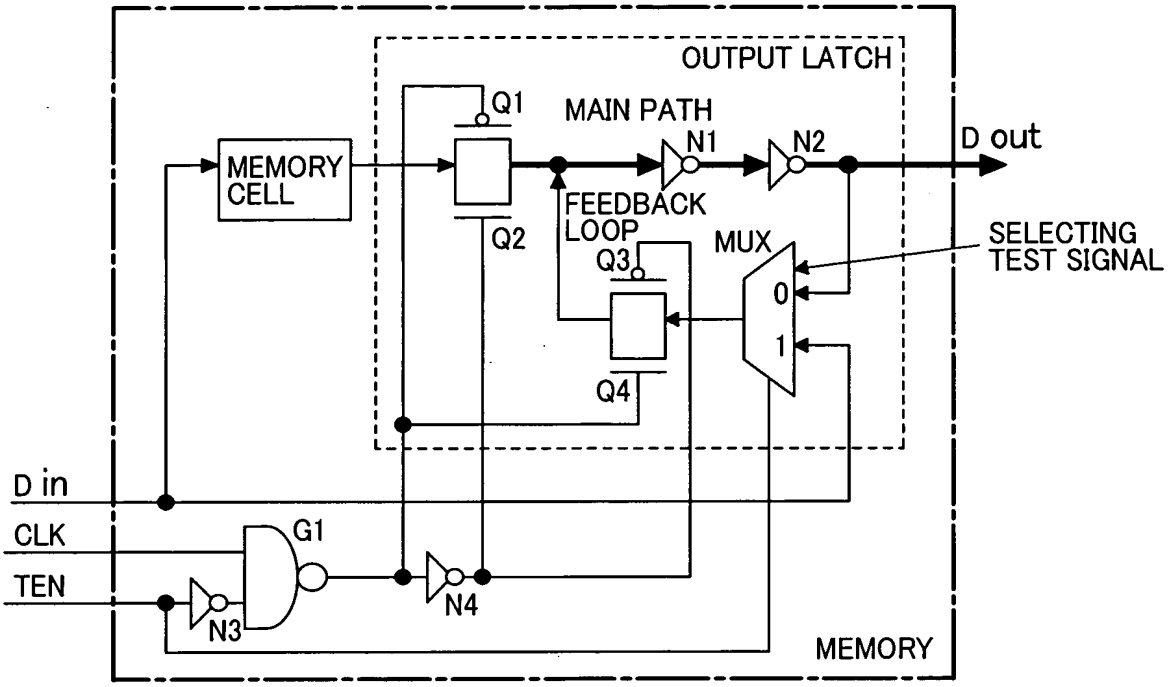
OUTPUT LATCH
Q1
MAIN PATH
N1
N2
D out
MEMORY CELL
FEEDBACK LOOP
Q2
MUX
Q3
SELECTING TEST SIGNAL
0
1
Q4
D in
CLK
G1
TEN
N3
N4
MEMORY

FIG.2

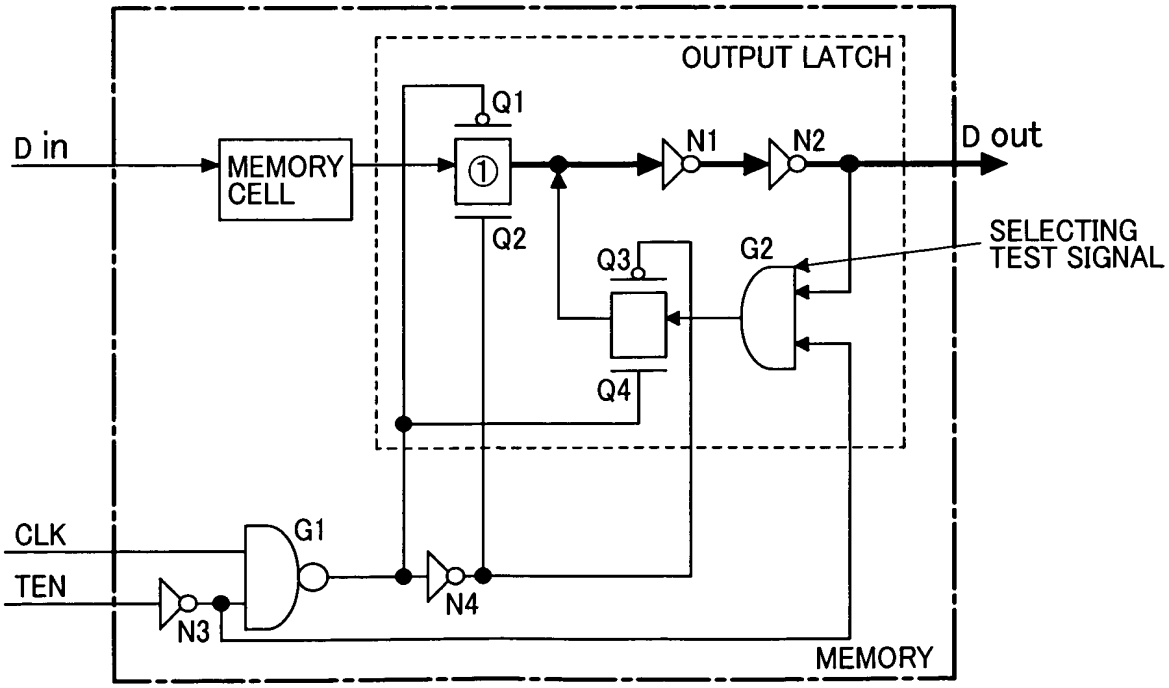
OUTPUT LATCH
Q1
D in
MEMORY CELL
①
N1
N2
D out
Q2
Q3
G2
SELECTING TEST SIGNAL
Q4
CLK
G1
TEN
N3
N4
MEMORY

FIG.3

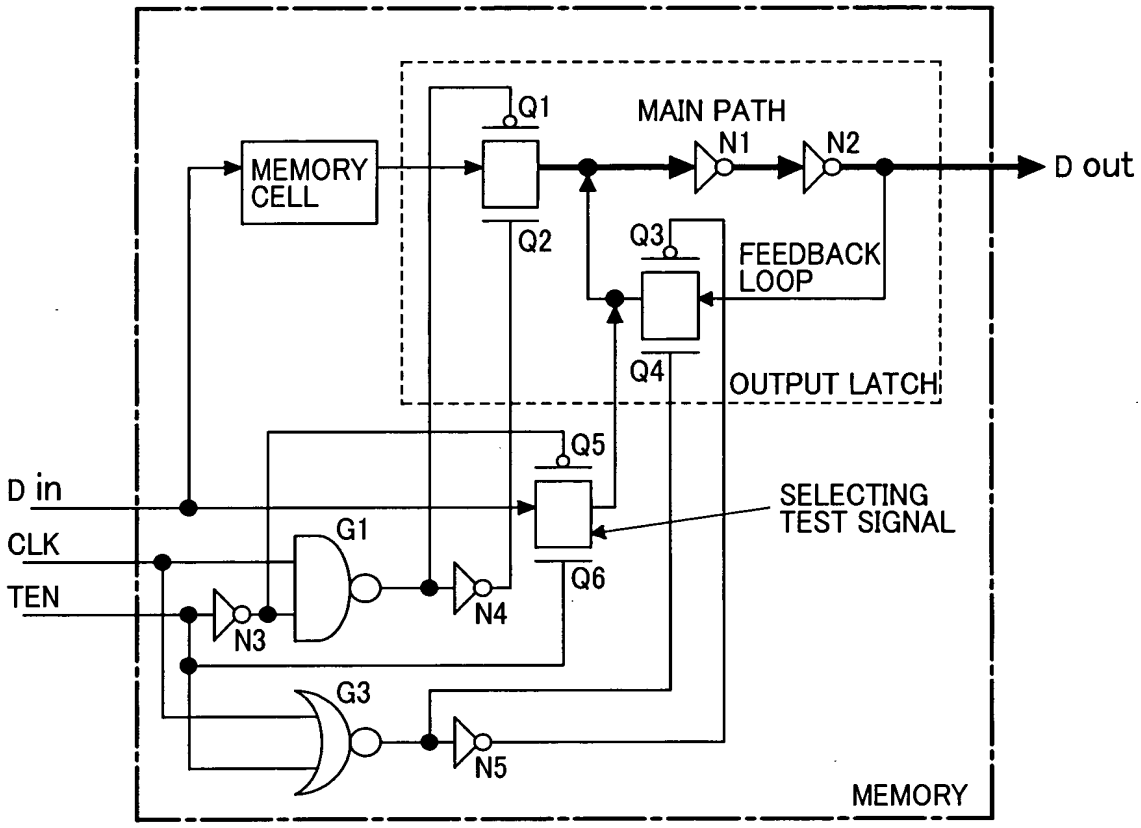
MEMORY CELL
Q1
MAIN PATH
N1
N2
D out
Q2
Q3
FEEDBACK LOOP
Q4
OUTPUT LATCH
Q5
D in
CLK
TEN
G1
N3
N4
Q6
SELECTING TEST SIGNAL
G3
N5
MEMORY

FIG.4

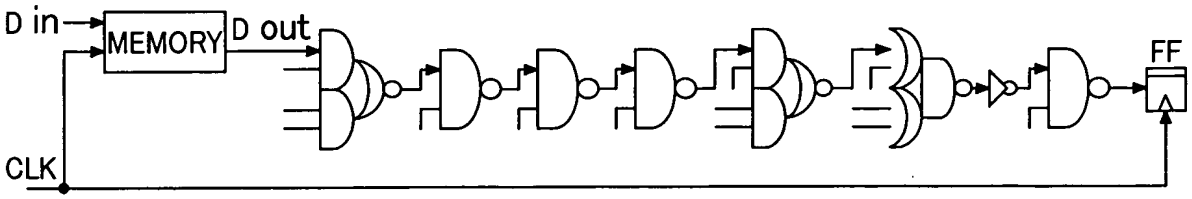
D in
MEMORY
D out
FF
CLK

FIG.5

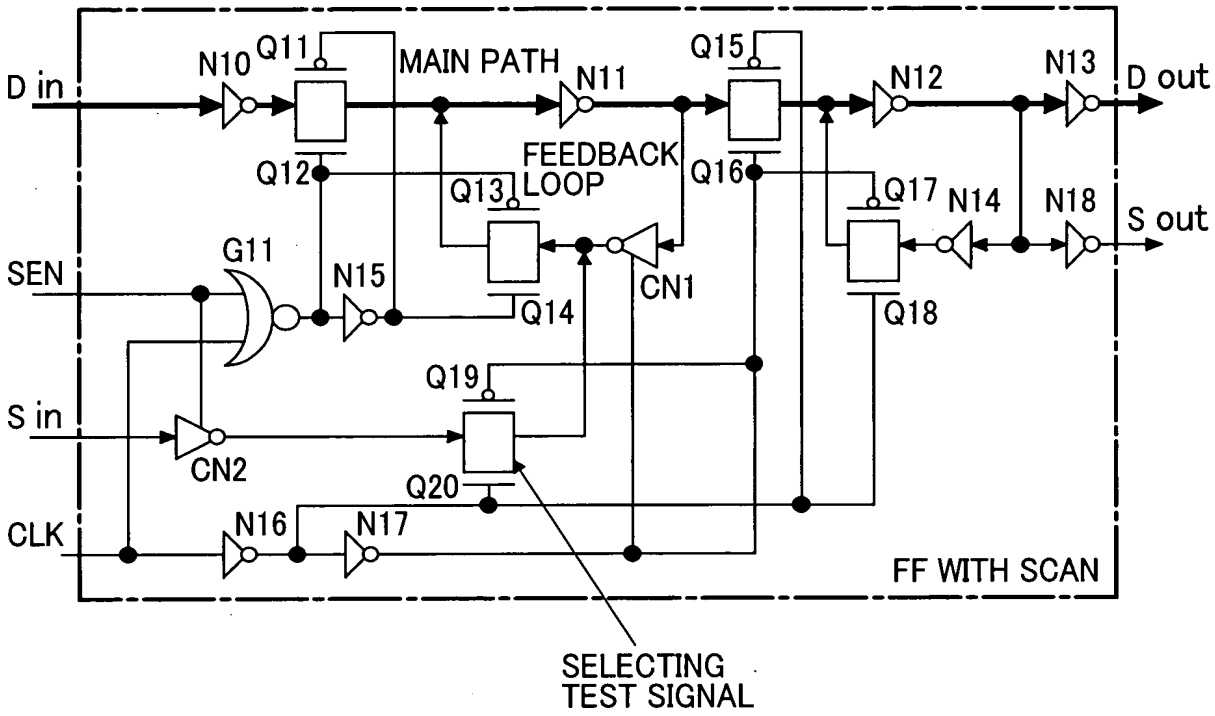
D in
N10
Q11
MAIN PATH
N11
Q15
N12
N13
D out
Q12
FEEDBACK
LOOP
Q13
Q16
Q17
N14
N18
S out
SEN
G11
N15
Q14
CN1
Q18
Q19
S in
CN2
Q20
CLK
N16
N17
FF WITH SCAN
SELECTING
TEST SIGNAL

FIG.6

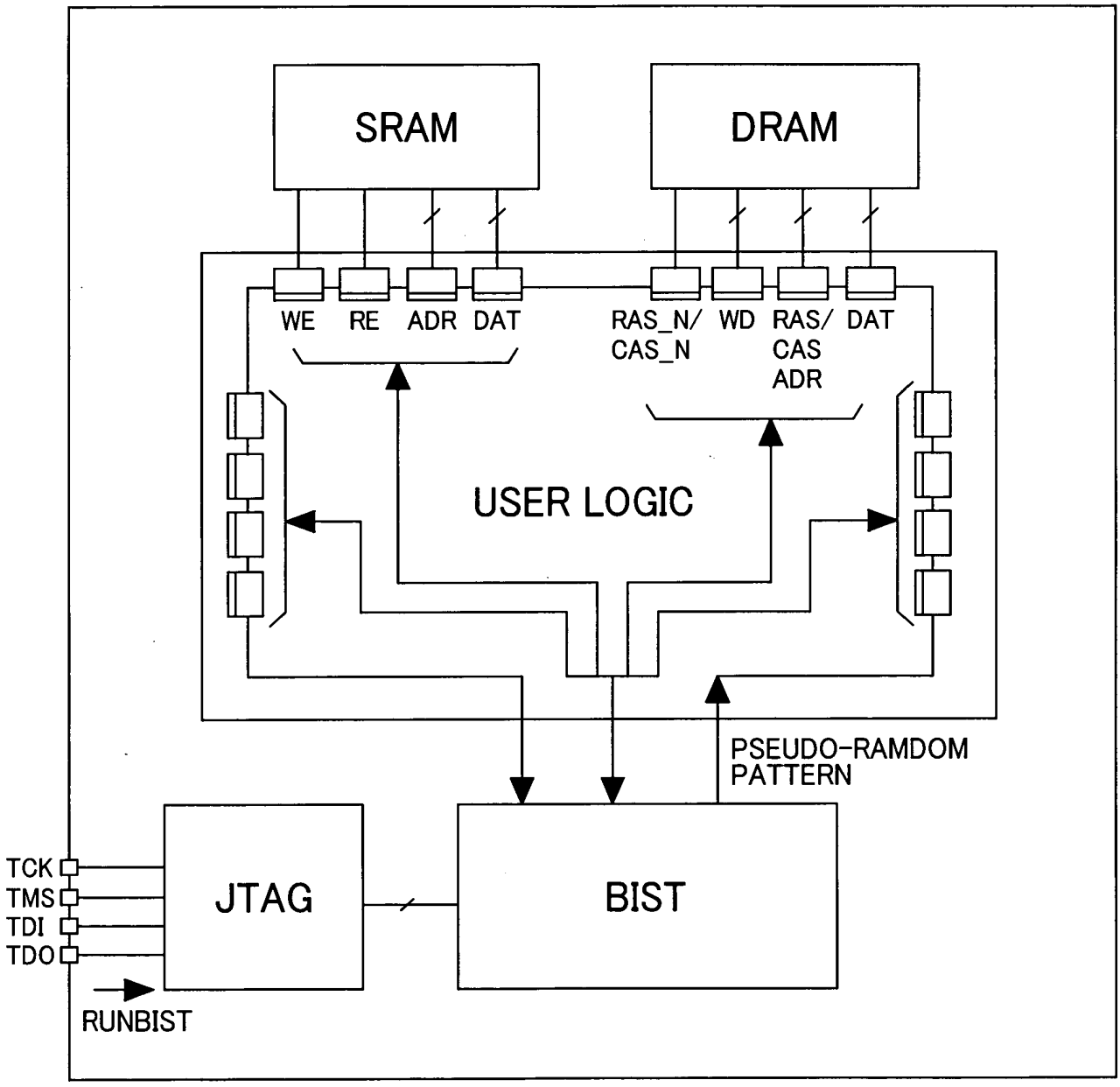
SRAM
DRAM
WE
RE
ADR
DAT
RAS_N/
CAS_N
WD
RAS/
CAS
ADR
DAT
USER LOGIC
PSEUDO-RAMDOM
PATTERN
TCK
TMS
TDI
TDO
JTAG
BIST
RUNBIST

FIG.7A

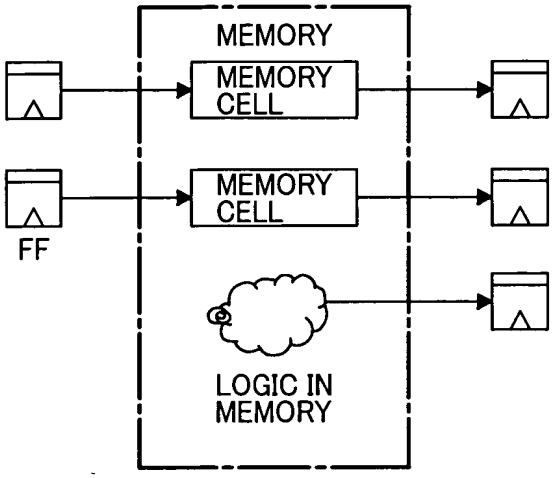

FIG.7B

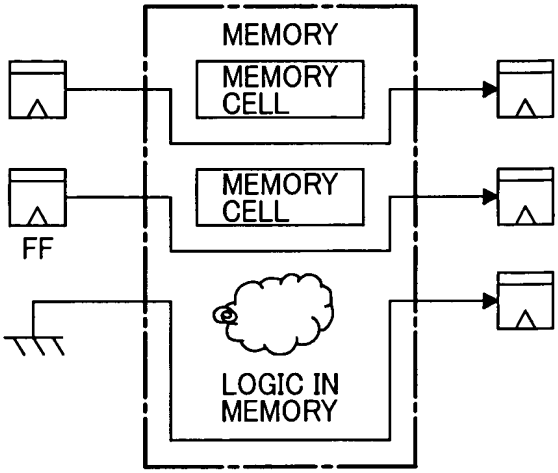

FIG.8